

ISL54224IRTZEVAL1Z Evaluation Board User Manual

Description

The ISL54224IRTZEVAL1Z evaluation board is designed to provide a quick and easy method for evaluating the ISL54224 USB Switch IC.

The ISL54224 device is a unique IC. To use this evaluation board properly requires a thorough knowledge of the operation of the IC. See the [ISL54224 datasheet](#) for an understanding of the functions and features of the device. Studying the device's truth-table along with the pin configuration diagram on page 2 of the datasheet is the best way to get a quick understanding of how the part works.

The ISL54224IRTZEVAL1Z evaluation board is shown in Figure 1. The ISL54224 TDFN IC is soldered onto the center of the evaluation board and is designated as U1.

The evaluation board includes USB connectors, banana jacks, and toggle switches that allow the user to easily interface with the IC to evaluate its functions, features, and performance. For example, with the board properly powered and configured as shown in Figure 2, the user can control the logic pins with toggle switches, S1 (SEL) and S2 (OE/ALM). These switches allow the user to switch between the two high-speed USB devices while connected to a single USB host (computer).

In a typical application, the ISL54224 dual SPDT device is used to select between two different USB transceiver sections of a media player. Logic control from a microprocessor determines which section to connect to the computer. The following sequence could be used to change channels:

1. A signal is sent to take the OE/ALM pin low, which opens all switches. The off-isolation of the ISL54224 device allows the present active channel to properly disconnect from the computer.
2. The SEL pin is set to select the other USB channel.
3. The OE/ALM pin is taken high to close the switches, which makes the connection between the computer and the other USB section of the player.

This application note guides the user through configuring and using the ISL54224IRTZEVAL1Z evaluation board to evaluate the ISL54224 device.

Features

- Standard USB Connectors
- Banana Jacks for Power, Ground, V_{BUS} and Logic Connections
- Toggle Switches for Easy Control of Logic Pins
- Jumpers to Allow a USB Device to Get Its V_{BUS} Voltage from the Host Controller
- Jumper to Connect a 100k Ω Pull-up Resistor from the OE/ALM Pin to VDD
- Convenient Test Points and Connections for Test Equipment

ISL54224IRTZEVAL1Z Evaluation Board

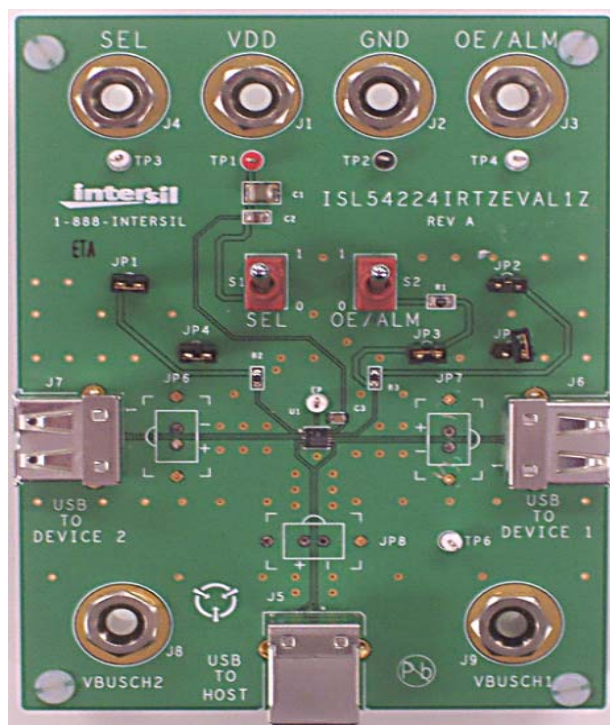


FIGURE 1. ISL54224IRTZEVAL1Z EVALUATION BOARD

Board Architecture/Layout

The basic layout of the evaluation board is as follows (see Figure 1 and “ISL54224IRTZEVAL1Z Board Schematic” on page 5).

- Power and ground connections are at the banana jacks (J1 and J2) at the top of the board.
- Logic connections SEL and OE/ALM are at the top of the board at banana jacks J4 and J3. They can also be accessed by using the toggle switches, S1 and S2, located in the upper center of the board. To use the toggle switches, jumpers JP1 and JP2 must be installed. To control the logic through banana jacks J4 and J3, the JP1 and JP2 jumpers should not be populated.
- The OE/ALM pin is an open-drain connection. It should be pulled high through an external 100k Ω pull-up resistor. The evaluation board has a 100k Ω pull-up resistor (R1) that can be connected between the OE/ALM pin and the VDD supply by installing a jumper at JP3.
- The USB connector, J5, located at the bottom of the board, provides a USB connection to an upstream host controller (computer).
- USB connectors J6 (USB TO DEVICE 1) and J7 (USB TO DEVICE 2), located on the right and left sides of the board, provide USB connections to downstream USB devices.
- Banana jacks J8 (VBUSCH2) and J9 (VBUSCH1) provide V_{BUS} voltage for USB devices. Optionally, V_{BUS} for a USB device can be connected to the host controller V_{BUS} through jumpers JP4 (Device 2) and JP5 (Device 1).
- The ISL54224 IC (U1) is located in the center of the board. The evaluation board has a Pin 1 indicator dot to show how the IC should be oriented on the evaluation board. The IC Pin 1 indicator dot should be aligned with the evaluation board Pin 1 indicator dot.

IC Power Supply

A DC power supply connected at banana jacks J1 (VDD) and J2 (GND) provides power to the ISL54224 IC. The IC requires a 2.7VDC to 5.25VDC power supply for proper operation. The power supply should be capable of delivering 100 μ A of current.

V_{BUS} Power Supply

A DC power supply connected at banana jacks J9 (VBUSCH1) and J8 (VBUSCH2) provides the V_{BUS} voltage required by the USB devices. The devices require a DC power supply in the range of 4.4V to 5.25V for proper operation. The power supply should be capable of delivering 100mA of current.

The J8 banana jack is connected to the VBUS pin of the J7 “A” type USB receptacle. The J9 banana jack is connected to the VBUS pin of the J6 “A” type receptacle.

V_{BUS} voltage can be provided from the USB host controller (computer) by installing a jumper at either JP4 or JP5.

With a jumper at JP4, the V_{BUS} voltage from J5 (USB TO HOST) gets routed to the J7 connector (USB TO DEVICE 2). With this jumper installed, no DC supply should be connected at the J8 (VBUSCH2) banana jack.

With a jumper at JP5, the V_{BUS} voltage from J5 (USB TO HOST) gets routed to the J6 connector (USB TO DEVICE 1). With this jumper installed, no DC supply should be connected at the J9 (VBUSCH1) banana jack.

Logic Control

The state of the ISL54224 device is determined by the voltage at the SEL pin and the OE/ALM pin. Access to the SEL pin is through the banana jack, J4 (SEL), or the toggle switch, S1 (SEL). Access to the OE/ALM pin is through the banana jack, J3 (OE/ALM), or the toggle switch, S2 (OE/ALM). To use the toggle switches to control the logic, jumpers should be installed at JP1 and JP2. Remove the jumpers to control the logic through the banana jacks.

A jumper installed at JP3 connects a 100k Ω resistor between the OE/ALM pin and VDD.

If SEL is driven low (to ground), OE/ALM = High (pulled up to VDD), and signal voltage is 0V to 3.6V, the high-speed (HS) channel 1 switches will be ON. In this state, the USB host controller (computer) connected at J5 is connected through to the USB device connected at J6, and data can be transmitted between the computer and the device.

If SEL is driven high, OE/ALM = High (pulled up to VDD), and signal voltage is 0V to 3.6V, the high-speed (HS) channel 2 switches will be ON. In this state, the USB host controller (computer) connected at J5 is connected through to the USB device connected at J7, and data can be transmitted between the computer and the device.

If OE/ALM = Low, all switches are OFF. Neither device is connected through to the host controller. OE/ALM can be driven low or is internally driven low by the ISL54224 IC in an overvoltage condition (signal is >3.8V or <-0.5V).

In a typical application, the ISL54224 dual SPDT device is used to select between two different USB transceiver sections of a media player. Logic control from a microprocessor determines which section to connect to the computer. To change channels, the following sequence could be followed:

1. A signal from the microprocessor is sent to take the OE/ALM pin low, which opens all switches. The off-isolation of the ISL54224 device allows the present active channel to properly disconnect from the computer.
2. The microprocessor drives the SEL pin to select the other USB channel.
3. The OE/ALM pin is allowed to go high by the microprocessor, which closes the switches and makes the connection between the computer and the other USB section of the player.

USB Connections

A “B” type USB receptacle labeled “USB TO HOST” (J5) is located on the bottom of the board. This receptacle should be connected, by a standard USB cable, to the upstream USB host controller, which is usually a PC computer or hub. When this connection is made, the ISL54224 device connects the computer through to the USB device according to the voltage at the SEL logic control pin.

An “A” type USB receptacle labeled “USB TO DEVICE 1” (J6) is located on the right side of the board. A USB device can be

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plugged directly into this receptacle or through a standard USB cable.

An “A” type USB receptacle labeled “USB TO DEVICE 2” (J7) is located on the left side of the board. A USB device can be plugged directly into this receptacle or through a standard USB cable.

The USB switches are bi-directional, which allows the host (computer) and downstream USB device to both send and receive data.

High-Speed Switches

The four HSx switches (HSD1-, HSD1+, HSD2-, HSD2+) are bi-directional switches that can pass signals up to 3.6V with a V_{DD} supply voltage in the range of 2.7V to 5.25V.

When powered with a 2.7V supply, these switches have a nominal r_{ON} of 6.5Ω over the signal range of 0V to 400mV, with an r_{ON} flatness of 0.3Ω . The r_{ON} matching between the HSDx- and HSDx+ switches over this signal range is only 0.06Ω , ensuring minimal impact by the switches to USB high-speed signal transitions. As the signal level increases, the r_{ON} switch resistance increases. At a signal level of 3.3V, the switch resistance is nominally 12Ω .

The HSx switches are specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth, which allows them to pass USB high-speed signals with minimum edge and phase distortion and thus meet USB 2.0 high-speed signal quality specifications.

The HSx switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling.

The maximum normal operating signal range for the HSx switches is from 0V to 3.6V. For normal operation, the signal voltage should not be allowed to exceed this voltage range or to go below ground by more than -0.3V.

If a positive voltage of $>3.8V$ (Typ) to 5.25V, such as the USB 5V V_{BUS} voltage, gets shorted to one or both of the COM+ and COM- pins, or if a negative voltage of $<-0.5V$ (Typ) to -5V gets shorted to one or both of the COM pins, the ISL54224 overvoltage protection (OVP) circuitry is activated. OVP allows the device to detect the overvoltage condition and open the SPDT switches to prevent damage to the USB downstream transceivers connected at the signal pins (HS1D-, HS1D+, HS2D-, HS2D+).

The OVP and power-off protection circuitry allow the COM pins (D-, D+) to be driven up to 5.25V while the V_{DD} supply voltage is in the range of 0V to 5.25V. In this condition, the part draws $<100\mu A$ of I_{COMx} and I_{DD} current and causes no stress to the IC. In addition, the SPDT switches are OFF and the fault voltage is isolated from the other side of the switch.

The OE/ALM pin gets internally pulled low whenever the part senses an overvoltage condition. The pin must be externally pulled high with a pull-up resistor and monitored for a low condition to determine when an overvoltage condition has occurred.

Board Component Definitions

Evaluation board components and their functions are shown in Table 1.

TABLE 1. BOARD COMPONENT DESCRIPTIONS

DESIGNATOR	DESCRIPTION
U1	ISL54224IRTZ IC
J5	“B” Type USB Receptacle
J6, J7	“A” Type USB Receptacle
J1	VDD Positive Connection
J2	VDD Negative Connection
J4	SEL Logic Control
J7	OE/ALM Logic Control
J8	V_{BUS} Voltage for High-speed Device 2
J9	V_{BUS} Voltage for High-speed Device 1
S1	SEL Toggle Switch
S2	OE/ALM Toggle Switch
JP6, JP7, JP8	D-/D+ Differential Probe Connection
JP4, JP5	Host Controller (Computer) V_{BUS} Jumper
JP1	Toggle Switch S1 (SEL) Jumper
JP2	Toggle Switch S2 (OE/ALM) Jumper
JP3	OE/ALM 100k Ω Pullup Jumper

Using the ISL54224IRTZEVAL1Z Evaluation Board (see Figure 2)

Lab Equipment

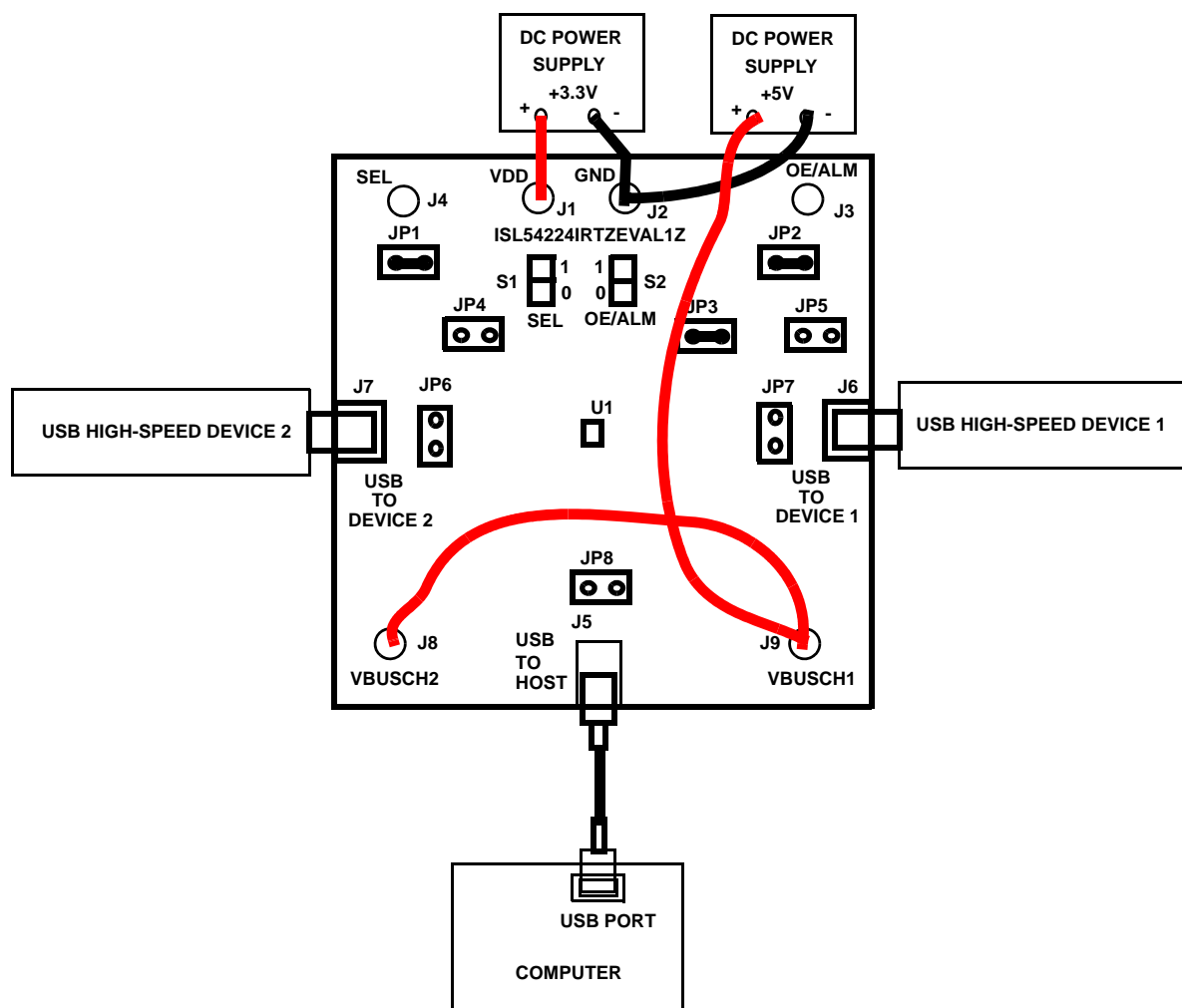
The equipment, external supplies, and signal sources needed to operate the board are:

1. +2.7V to +5V DC power supply
2. +5V DC power supply
3. Two high-speed USB devices (e.g., USB memory stick and MP3 player)
4. Computer with 2.0 high-speed USB port
5. Standard USB cable

Initial Board Setup Procedure

1. Install jumpers at JP1, JP2, and JP3. Remove jumpers from JP4 and JP5.
2. Attach the main evaluation board to a DC power supply at J1 (VDD) and J2 (GND). Put the positive terminal at J1 and the negative terminal at J2. The supply should be capable of delivering 2.7V to 5V and 100 μA of current. Set the supply voltage to 3.3V.
3. Connect a DC power supply at J8 (VBUSHCH2) and J9 (VBUSCH1). Put the positive terminals at J8 and J9 and the negative terminal at J2 (GND). The supply should be capable of delivering 5V and 100mA of current. Set the supply voltage to 5V. This supply provides 5V at the V_{BUS} pin of the USB “A” type connectors, J6 and J7.

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Note: For Device 1 to get VBUS from the computer through the J5 connector, disconnect the 5V supply from J9 and populate jumper JP5. For Device 2 to get VBUS from the computer through the J5 connector, disconnect the 5V supply from J8 and populate jumper JP4.

FIGURE 2. BASIC EVALUATION TEST SETUP BLOCK DIAGRAM

4. Connect one high-speed USB device at USB connector, J6, and the other high-speed USB device at USB connector, J7. These connectors are located on the left and right sides of the evaluation board.
5. Drive the OE/ALM control pin low to open all switches of the ISL54224 IC by putting toggle switch, S2 (OE/ALM), in the down position.
6. Connect the USB cable from the host (computer) to the USB "B" type receptacle, J5 (USB TO HOST).
4. To disconnect USB Device 1 from the computer, take the OE/ALM pin low by putting toggle switch, S2 (OE/ALM), in the down position.

High-Speed Channel 1 Operation

1. Apply a logic LOW to the SEL pin by putting toggle switch, S1 (SEL), in the down position.
2. Apply a logic HIGH to the OE/ALM pin by putting toggle switch, S2 (OE/ALM), in the up position.
3. You should now be able to send and receive data between the computer and USB Device 1, connected at J6.

High-Speed Channel 2 Operation

1. Apply a logic HIGH to the SEL pin by putting toggle switch, S1 (SEL), in the up position.
2. Apply a logic HIGH to the OE/ALM pin putting toggle switch, S2 (OE/ALM), in the up position.
3. You should now be able to send and receive data between the computer and USB Device 2 connected at J7.

Test Points

The board has various test points to allow the user to connect probes to make measurements. The test points are described in Table 2.

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TABLE 2. TEST POINTS

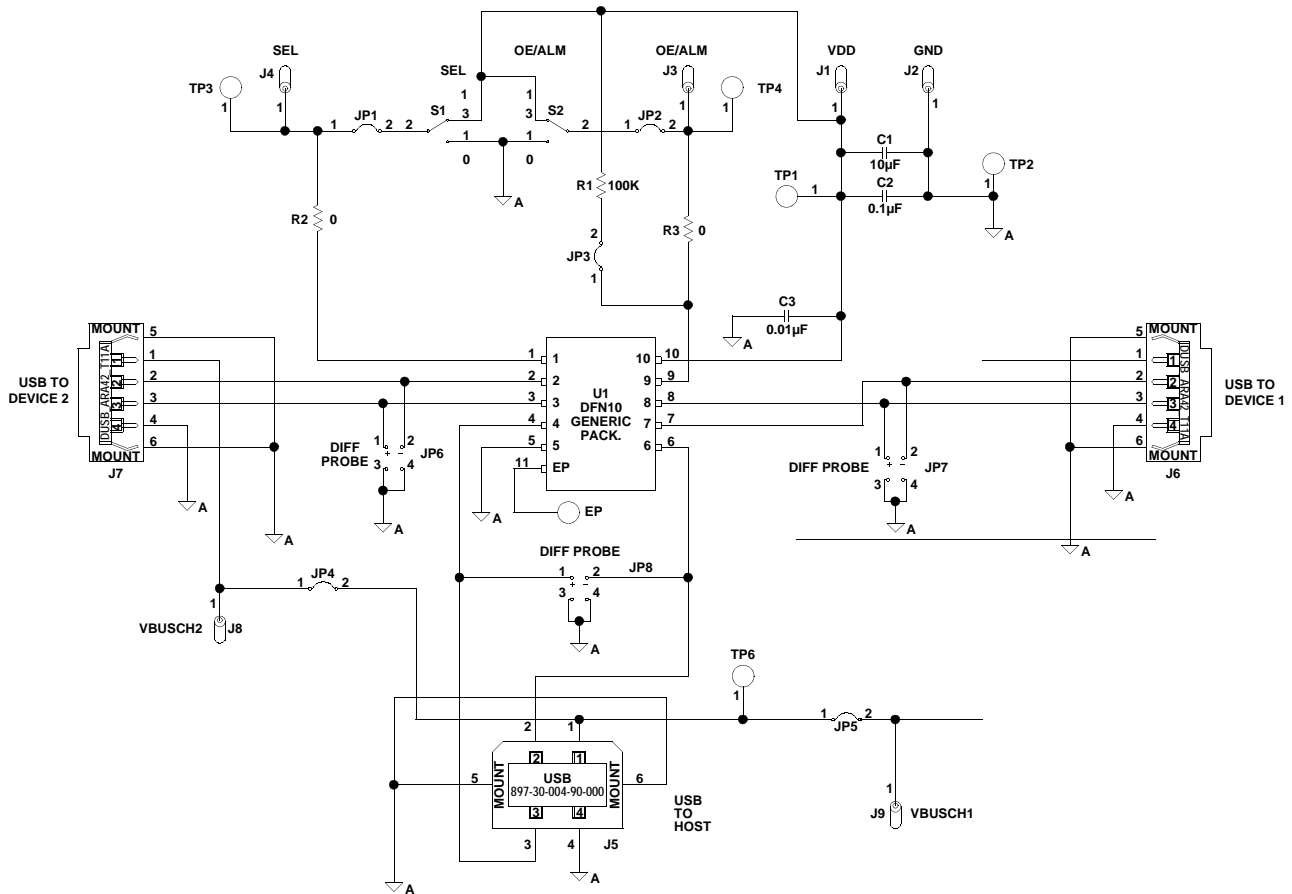
DESIGNATOR	DESCRIPTION
TP1	V _{DD} test point
TP2	Ground test point
TP3	SEL test point
TP4	OE/ALM test point
TP6	VBUS from Pin 1 of Connector J5 test point
JP8	D-/D+ differential probe connection; COM side of switch
JP7	D-/D+ differential probe connection; Device 1 side of switch
JP6	D-/D+ differential probe connection; Device 2 side of switch

You can observe the D- and D+ USB signal of high-speed Channel 1 on an oscilloscope or other test equipment by connecting a differential probe at JP7.

You can observe the D- and D+ USB signal of high-speed Channel 2 on an oscilloscope or other test equipment by connecting a differential probe at JP6.

You can observe the D- and D+ USB signal at the COM side of the switch on an oscilloscope or other test equipment by connecting a differential probe at JP8.

ISL54224IRTZEVAL1Z Board Schematic



Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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